Layouts For The Shuffle-exchange Graph And Lower Bound Techniques For VLSI (MIT/LCS/TR) By Frank Thomson Leighton

By Frank Thomson Leighton

Permutation-exchange graphs that emulate the binary cube Kleitman, D., Leighton, F. T., Lepley, M., and Miller, G. L., New layouts for the shuffle-exchange graph.
http://link.springer.com/article/10.1007/BF01744440

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http://www.academia.edu/1342614/Existence_of_Nash_equilibria_in_selfish_routing_problems

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http://www.dtic.mil/cgi-bin/GetTRDoc?Location=U2&doc=GetTRDoc.pdf&AD=ADA121538

new lower bound techniques for vlsi: mit-lcs-tm-227: layouts for the shuffle-exchange graph based on the complex plane diagram: mit-lcs-tm-221: leighton, frank
http://publications.csail.mit.edu/lcs/viewpubs.php?permit_indexing&cat=tm&sort=docnum&count=2000

Complexity Issues in VLSI: Optimal Layouts for the Shuffle-Exchange Graph and Other Networks (Foundations of Computing) [Frank Thomson Leighton] on Amazon.com. *FREE
http://www.amazon.com/Complexity-Issues-VLSI-Shuffle-Exchange-Foundations/dp/0262621789

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http://www.ibiblio.org/pub/linux/docs/LSM/LSM.2002-04-01.gz

Received: from charon.cwi.nl by theory.lcs.mit.edu (5 of Shuffle Inequalities, S. L in a Parallel Algebraic Graph Grammars
http://homepages.cwi.nl/~bertl/concurrency/archive/concurrency-1995

Accession Number : ADA121538. Title : Layouts for the Shuffle-Exchange Graph and Lower Bound Techniques for VLSI. Descriptive Note : Doctoral thesis,
http://www.dtic.mil/docs/citations/ADA121538

Abstract: This paper describes a technique for producing a VLSI layout of the shuffle-exchange graph. It is based on the layout procedure which lays out a graph by
http://www.academia.edu/2435048/A_layout_for_the_shuffle-exchange_network

Complexity Issues in VLSI. In particular, it describes optimal layouts for the shuffle-exchange graph, one of the best known networks for parallel computation.
https://mitpress.mit.edu/index.php?q=books/complexity-issues-vlsi

SIAM Journal on Algebraic Discrete Methods. Article Tools. Add to my favorites. Layouts for the Shuffle-Exchange Graph Based on the Complex Plane Diagram.
http://epubs.siam.org/doi/abs/10.1137/0605021

3. The Shuffle-Exchange Graph The shuffle-exchange graph on n vertices is defined only when n is a power of two. Each of the n 2k vertices can be identified with an
http://people.csail.mit.edu/cel/resume/papers/Layout-for-ShuffleExch.pdf

The shuffle exchange graph is one of the best structures known for parallel An Asymptotically Optimal Layout for the Shuffle-Exchange Graph DANIEL
http://www.sciencedirect.com/science/article/pii/0022000083900053

found that the optimal shuffle-exchange (SE) graph layout from [9] applied to the implementation of Viterbi decoders
http://orbit.dtu.dk/fedora/objects/orbit:15811/datastreams/file_3800388/content

MIT LCS Technical Memo TM-116, Frank Thomson Leighton, we present several new layouts for the shuffle-exchange graph,
http://dl.acm.org/ft_gateway.cfm?id=802492&type=pdf&coll=portal&dl=ACM

This paper studies linear layouts of generalized hypercubes, Complexity Issues in VLSI: Optimal Layouts for the Shuffle-Exchange Graph and Other Networks.
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Frank Thomson Leighton; Massachusetts Institute of Technology, A new divide-and-conquer framework for VLSI graph layout is introduced.
http://www.sciencedirect.com/science/article/pii/0022000084900710
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http://www.amazon.com/Frank-Thomson-Leighton/e/B001HQ5T70

MIT-LCS-TR-695: Frank, Formal Specification Techniques for Promoting Software A FRAMEWORK FOR SOLVING VLSI GRAPH LAYOUT PROBLEMS: MIT-LCS-TR-305: Bhatt, S.N.
http://publications.csail.mit.edu/lcs/viewpubs.php?permit_indexing&cat=tr&sort=docnum&count=2000

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http://dl.acm.org/citation.cfm?id=1109557.1109670&preflayout=flat

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